Reply To Examiner's Remarks

Claims 1-3, 5, 7-14 and 16, as amended, are presented for consideration.

The Examiner rejects claims 1-3, 5, 7-16 under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement, noting that the recited claims clauses "non-electrically conductive layer," "organometallic," "etching process," in claim 1, and "non-conductive material" in claim 15 are not described in the original specification. These claims clauses are deleted herein.

The Examiner also asserts that the claims clause "to prevent migration of the MeNW material" in claim 1 does not appear in the original specification. Use of a diffusion barrier 23 (e.g., of TiN or TaN) to prevent metal diffusion of the underlying conductive layer material to adjacent material, is discussed at page 5, lines 9-13, claims 1, 6 and 7 of the original specification, and Figure 1A, step 12. Claim 1 is amended to recite

> "providing a diffusion barrier of a selected barrier material as a thin coating surrounding a side wall of the at least two MeNWs and overlying exposed portions of the conductive layer, to prevent migration of the conductive layer material;"

The Examiner rejects claims 1-3, 5, 7-14 and 16 under 35 U.S.C. 102 as anticipated by the disclosures in published U.S. patent application no. 2003/0189202, filed by Li et al (the "Li PPA"), published patent application no. 2001/0030366, filed by Nakano et al (the "Nakano et al PPA"), and published patent application no. 2004/0071951, filed by in (the "Jin PPA"), referred to collectively herein as "the cited references."

The Li et al PPA discloses methods for fabrication of nanowire devices in which: (1) one or more electrodes is set down on a conducting substrate; (2) a pattern of one or more nanowire growth catalyst sites is provided on each

electrode; (3) one or more nanowires is grown on each catalyst site; (4) each nanowire is connected to a selected electrical source at an "exposed end" of the nanowire; (5) each nanowire is surrounded by interstitial electrical insulation, extending between adjacent nanowites, to insulate the nanowires from each other; (6) each nanowire is planarized at an exposed end to expose a tip of a nanowire above the insulation material (Figures 4a-4f). The Li et al PPA does not disclose or suggest

> "providing a diffusion barrier of a selected barrier material as a thin coating surrounding a side wall of the at least two MeNWs and overlying exposed portions of the conductive layer, to prevent migration of the MeNW material"

as recited in claim 1 of the subject patent application.

The Jin PPA discloses a high density information storage medium and fabrication method, which uses a periodic array of vertically aligned carbon nanotubes ("CNTs") for such storage. Each CNT is coated with, or filled with, a selected magnetic material (Fe, Ni, Co), interstitial gaps between adjacent coated CNTs are filled with a non-magnetic material, such as a metal or alloy (Al, Ti, Si, Cu, Mo or Cr or alloy thereof) and the array of coated CNTs and gap material are planarized to expose tips of the coated or filled CNTs (Figure 3). Optionally, as indicated in Figures 5B and 5C, the nanowire surfaces are oxidized, and subsequently subjected to a reducing atmosphere. Figures 5(a), 5(b) and 5(c) of the Jin et al PPA, and paragraphs 0044, 0045 and 0046 of the published specification, disclose that the nanowires 12 (used for high density recording according to the PPA) are provided with an oxidized surface 50, by heating in a high temperatu1re, oxygen-rich environment. According to paragraph 0045, this oxidized surface serves to decrease the diameter of the magnetic core -- but no other purpose for provision of the oxidized surface is given.

The Nakano PPA discloses a method for producing a semiconducting system, using a protective coating of TaN or TiN. Paragraph 0012 of the Nakano et al PPA notes that SiN is insulating and has been used as a wire protective film, with a high specific dielectric constant. The paragraph also notes that nitrides such as Ti_uN_v, Ta_uN_v and W_uN_v have been used as a high melt point wire protective film and to avoid short circuiting between wires. No other purpose for provision of the wire protective film is given in the Nakano et al PPA.

Claim 1, as amended, and the discussion in the specification of the subject patent application, recite that a diffusion barrier of a selected barrier material as a thin coating surrounding a side wall of the at least two MeNWs and overlying exposed portions of the conductive layer is provided, to prevent migration of the conductive layer material into adjacent material. Material chosen as a wire protective film or to decrease a diameter of a magnetic core for a memory element, would not necessarily behave properly as a diffusion barrier, and conversely. Thus, it would not have been obvious to provide a diffusion barrier, for the purpose recited in amended claim 1, from the relevant portions of the disclosures in the Li et al PPA, the Jin et al PPA and/or the Nakano et al PPA.

The Applicants believe that claim 1, as amended, of the subject patent application is allowable over the disclosures in the cited references. Claims 3-5, 7-14 and 16, as amended, depend upon amended claim 1 and are believed to be allowable if amended claim 1 is allowable. The Applicants request that the Examiner pass the application, including claims 1, 3-5, 7-14 and 16, as amended, to issue as a U.S. patent.

Respectfully Submitted,

John Schipper

Date: 06 October 2006

John Schipper

Patent representative for Applicants

Reg. No. 26994